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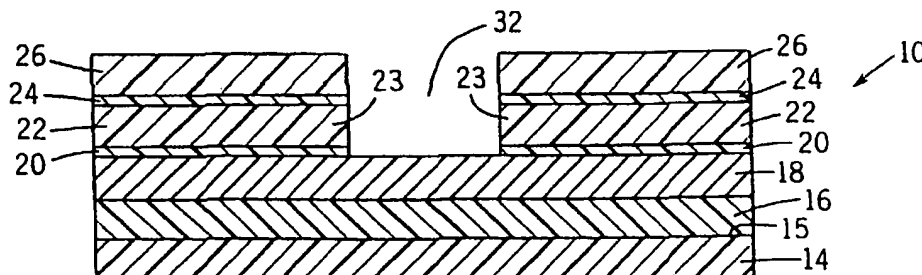
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For two-letter codes and other abbreviations, refer to the "Guid-
ance Notes on Codes and Abbreviations" appearing at the begin-
ning of each regular issue of the PCT Gazette.

(54) Title: PHOTORESIST REMOVAL PROCESS USING FORMING GAS PLASMA



(57) Abstract: An integrated circuit and a method of removing photoresist is described. The process described uses a low oxygen gas or non-oxygen forming gas plasma that removes the photoresist (26) and provides a protective surface layer over the low-k dielectric material (22) exposed at sidewalls of etched via (32). The low-k dielectric material (22), preferably HSQ, BCB or the like, is part of a dielectric stack (20, 22, 24). After exposure to the gas plasma, preferably comprising H₂+N₂+CF₄, the integrated circuit is subjected to solvent to remove residual photoresist, and a degas step.

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PHOTORESIST REMOVAL PROCESS USING FORMING GAS PLASMA

Technical Field

The invention relates to the fabrication of integrated circuits and more particularly to removing photoresist from an integrated circuit by using a non-oxygen gas or low oxygen gas plasma process.

Background Art

In very large scale integrated (VLSI) circuit devices, several wiring or metal layers are required to connect together the active or passive elements in a VLSI semiconductor chip. The interconnection structure consists of thin conductive lines separated by insulation (silicon dioxide) in one layer or level and connected to elements of the semiconductor chip or to a similar layer in another level. Vias or studs extend through the insulation and can be connected to contacts associated with the elements of the semiconductor chip. Connections between levels or layers and between layers and the elements of the semiconductor chip are then made. Conventional ultra-large scale integrated (ULSI) circuit devices can include five or more layers.

The interconnection structure associated with VLSI and ULSI circuits is similar to a transmission line in that there is a propagation delay of the signals being transmitted in these wiring layers. The delay is referred to as RC delay because it generally relates to the resistance (R) of the material of the wire and the capacitance (C) between adjacent wires.

With the trend of higher and higher levels of integration in integrated circuits (ICs), the space or gap (e.g., the thickness between the conductive lines or layers) is becoming extremely narrow, such as about 0.5 microns and smaller. Such a narrow space or gap between conductive lines increases the capacitance and places greater demands on the insulating properties of the insulation between such conductive lines. Capacitance (C) is the product of dielectric constant (k) of the insulating material times the area (A) of the opposing faces of the conductive line divided by the distance (D) between the conductive lines $\left(C = \frac{kA}{D} \right)$. With a decrease in distance (D), the capacitance (C) increases. Since signal delay of signals transmitted on the conductive line is controlled by the RC constant, an increase in capacitance (C) degrades the performance of the integrated circuit.

Thus, it is desirable to replace traditional silicon dioxide (SiO₂) insulative materials in multi-level interconnect devices with dielectric materials having low dielectric constants (hereinafter referred to as low-k dielectric materials). A disadvantage to using low-k dielectric materials is that traditional photoresist removal processes (e.g., ashing and solvent cleaning) causes degradation of most low-k dielectric materials. For example, photoresist removal on low-k dielectric materials, such as, hydrogen silsesquioxanes (HSQ), spin on glass (SOG), benzocyclobutene (BCB), etc., causes the dielectric constant (k) to increase. Furthermore, the conventional solvent cleaning of the integrated

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circuit after the ashing process typically causes further degradation of low-k dielectrics and causes increases in dielectric constant k.

Thus, there is a need and desire for a method of producing integrated circuits, including VLSI and ULSI circuits, that maintains the integrity of low-k dielectric materials during the ashing and solvent cleaning process associated with photoresist removal. Further, there is a need and desire for a method of producing integrated circuit devices that uses a non-oxygen gas (O₂) or trace O₂ forming gas plasma process that creates a protective surface layer and removes photoresist with a relatively high ashing rate. Further still, there is a need and desire for a method of producing an integrated circuit device that uses a high temperature and high vacuum degassing process to remove trace amounts of photoresist and eliminates moisture on the surface of the integrated circuit device while preserving the integrity of the low-k dielectric material.

Disclosure of the Invention

The present invention relates to a method of photoresist removal from an integrated circuit wafer. The method includes exposing the wafer to a plasma. The forming gas of the plasma is substantially free of oxygen gas (O₂) and removes photoresist from the integrated circuit wafer. The method also includes removing the remaining photoresist from the wafer using a solvent and degassing the integrated circuit wafer.

The present invention also relates to a method of photoresist removal from an integrated circuit wafer. The method includes providing an integrated circuit having a layer of photoresist overlying a dielectric stack. The method also includes placing the integrated circuit in a substantially pure plasma to remove photoresist from the integrated circuit wafer.

The present invention still further relates to an integrated circuit. The integrated circuit includes a dielectric stack having a first insulative layer, a second insulative layer and a third insulative layer, the second insulative layer being a low-k dielectric layer between the first insulative layer and the third insulative layer. A via extends through the dielectric stack and the lateral sides of the second layer of the dielectric stack includes a protective layer.

Brief Description of the Drawings

The invention will hereafter be described with reference to the accompanying drawings, wherein like reference numerals denote like elements in the various drawings, and:

FIG. 1 is a cross sectional view of a portion of an integrated circuit having a top layer of photoresist;

FIG. 2 is a cross sectional view of the integrated circuit of FIG. 1 having some of the photoresist of FIG. 1 selectively removed;

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FIG. 3 is a cross sectional view of the dielectric stack illustrated in FIG. 2 having a via etched through the dielectric layers; and

FIG. 4 is a cross sectional view of the integrated circuit of FIG. 3 depicting the integrated circuit with the photoresist removed.

Modes for Carrying Out the Invention

Referring to FIG. 1, a portion of an integrated circuit wafer 10 is depicted. Integrated circuit wafer 10 includes a silicon substrate 14, a low-k dielectric layer 16, a conductive metal layer 18, an oxide layer 20, a low-k dielectric layer 22, an oxide layer 24, and a photoresist layer 26. Silicon substrate 14 is typically a single crystal silicon wafer having a thin layer of silicon dioxide on its outermost surface 15. Alternatively, substrate 14 may be a silicon dioxide (SiO₂) substrate, a gallium arsenide (GaAs) substrate, or other insulating materials.

Low-k dielectric layer 16 is deposited over silicon substrate 14. Low-k dielectric layer 16 is a thin layer of low-k material, having a thickness of approximately 200 Angstroms, or alternatively any suitable thickness. Low-k dielectric layer 16 may be a spin on deposit of materials such as HSQ, SOG, BCB or other suitable materials. The low-k dielectric materials are deposited using spin on deposit techniques in which the materials are dissolved in a solvent and spun on to integrated circuit wafer 10. Alternatively, chemical vapor deposition (CVD) techniques can be used or any other deposition techniques that are known to those of ordinary skill in the art of semiconductor fabrication. After thin layer of low-k dielectric 16 has been deposited over substrate 14, low-k dielectric 16 may be heat cured or in the alternative, low-k dielectric 16 may be electron beam cured or cured by any suitable manner known to those of ordinary skill in the art.

Conductive metal layer 18 is deposited over low-k dielectric layer 16. Conductive layer 18 may be deposits of aluminum (Al), copper (Cu), gold (Au), tungsten (W), or alloys including these metals or polysilicon. Conductive metal layer 18 may be deposited by evaporation methods, such as physical vapor deposition (PVD), sputtering or plating. Evaporation methods use heat and high-vacuum to cause vaporization of a metal source. The vaporized metal material condenses on the cooler wafer surface. Sputtering techniques are well known in the art and use a plasma to bombard a metal source. The dislodged metal molecules are then deposited onto the wafer.

After conductive metal layer 18 is deposited and patterned (when creating a subtractive metal interconnect structure as opposed to the damascene structure depicted in the figures), an optional oxide layer 20 is deposited utilizing for example a tetraethylorthosilane (TEOS) process or other suitable processes known to those of ordinary skill in the art. Alternatively, silicon dioxide or other suitable materials can be deposited as oxide layer 20.

Low-k dielectric layer 22 is then deposited over oxide layer 20, similar to low-k dielectric layer 16. A cap layer 24 (usually an oxide layer) is then deposited over low-k layer 22, similar to oxide layer 20. Layers 24, 22, and 20 form a dielectric stack. Alternatively, the dielectric

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stack may be a single insulating layer of low-k dielectric 22 or any suitable combination of dielectric layers.

Photoresist layer 26 is a layer of photoresist or mask material, which is a photo-sensitive material, that is applied over oxide layer 24 in a liquid state in relatively small quantities. The wafer is spun at approximately 3,000 RPMs spreading the photoresist material into a uniform layer, typically between 0.15 and 200 micrometers (μm) thick. Two types of photoresist may be used, the two types being negative photoresist and positive photoresist.

A negative photoresist causes unexposed portions of the photoresist to be removed leaving a "negative image". Negative photoresist is typically only capable of producing features down to about 2 μm . Most conventional semiconductor processes today use a positive resist where exposed portions are removed leaving a "positive image" of the masked pattern on the surface of the wafer.

Positive resists are more capable of producing the small size of modern device features which are typically below 1 μm but may be as small as 0.15 μm .

After photoresist layer 26 is deposited on oxide layer 24, photoresist layer 26 is masked. If a positive resist is used, the portions which are not to be removed are masked. The masked wafer is then exposed to high intensity ultra-violet light. The ultra-violet light causes the exposed photoresist to undergo a chemical change, becoming more acidic. Once the wafers have been developed by exposure, the wafers are etched either in an acid or base solution to remove (or strip) the exposed areas of the photoresist. The wafer is then heated at a low temperature which hardens the remaining photoresist 26. With reference to FIG. 2, this developing and stripping procedure leaves a pattern of channels 30 in the photoresist 26.

After the pattern of channels 30 has been created in the photoresist, an etching process, known to those of ordinary skill in the art, is used to create a via 32 (FIG. 3) through layers 24, 22, and 20. Via 32 can be created by dry etching. Via 32 will be used to create a post contact to interconnect conductive metal layer 18 with another layer of device 10, such as a layer (not shown) above layer 24.

Once layers 20, 22, and 24 have been etched to form via 32, photoresist 26 may be removed. According to the invention, ashing (or photoresist removal) is performed in a non-oxygen gas or trace oxygen forming gas plasma process. Wafer 10 is exposed to a high temperature plasma that selectively removes photoresist 26 without damaging conductive lines 18, oxide layer 20, low-k dielectric layer 22, or oxide layer 24. In a preferred embodiment of the present invention, the plasma used is non-oxygen forming gas plasma. For example, in a preferred embodiment a non-oxygen forming gas plasma may be used that contains up to 20% of combined hydrogen gas (H_2) and nitrogen gas (N_2). If photoresist layer 26 has a thickness on the order of 1 μm , wafer 10 should be exposed to the plasma for approximately 4-10 minutes at a temperature of 250-270°C to complete the photoresist removal. Alternatively, other plasma forming gasses may be used having either no O_2 or a trace amount of O_2 (less than 5%) and the exposure times and temperatures should be varied accordingly. For instance, plasmas that are suitable for use are plasmas that do not degrade the low-k properties in the dielectric layer. For instance, other plasma forming gasses that may be suitable are $\text{H}_2 + \text{N}_2 + \text{trace}$

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O₂ forming gasses, water (H₂O) vapor forming gasses, and H₂ + N₂ + CF₄ (carbon tetrafluoride) forming gasses, and any other O₂-less or low-O₂ forming gasses that do not substantially degrade low-k dielectric layer 22 and still provide an adequate ashing rate. Plasmas from forming gasses in this class may be characterized as substantially pure plasmas, i.e., plasmas having an O₂ content less than about 5% so that the oxygen does not cause reaction with the low-k dielectric which would substantially raise the k value thereof.

In a preferred embodiment of the present invention, it is also desirable for the plasma to create a protective layer on surface 23 of low-k dielectric material 22. The protective layer is created during exposure of layer 22 to the plasma. Exposure of low-k dielectric layer 22 to the conditions present during plasma ashing causes a physical or chemical change to surface 23 of low-k dielectric 22. This protective layer provides a protective block such that O₂ plasma photoresist ashing solvent and photoresist removal solvent does not easily penetrate the protective layer and further degrade the low-k dielectric layer. A thicker protective layer provides better protection from solvent attack of low-k dielectric layer 22. Therefore, low dielectric constants of layer 22 are maintained. If a pure O₂ plasma is used to remove photoresist layer 22, the low-k dielectric layer is degraded or removed.

After the photoresist has been removed using a low-O₂ or O₂-less plasma process, wafer 10 is deposited in a solvent that removes any remaining photoresist from wafer 10. As discussed earlier, exposing low-k dielectric layer 22 to many solvents will cause degradation of low-k dielectric layer 22 and will cause a significant rise in the dielectric constant (k) (as the dielectric constant of water is 85). Therefore, it is desirable to use a photoresist ashing process, as described above, that provides a protective layer over low-k dielectric layer 22 in advance of the solvent cleaning process.

After the cleaning process has removed the majority of remaining photoresist, a degassing process is used to remove any trace photoresist and eliminate any moisture. The degassing process includes placing integrated circuit wafer 10 in a vacuum, such that the solvent and any trace photoresist is evaporated. Furthermore, the degassing process may be accomplished by exposing integrated circuit wafer 10 to high temperature (i.e., heating integrated circuit wafer 10) alone or in combination with exposing integrated circuit wafer 10 to a vacuum. The resulting device 10 is depicted in FIG. 4 having a via 32 extending through insulative layers 24, 22, and 20 and being terminated at conductive metal layer 18, where a post contact may be deposited in a next processing step.

Experimental results have provided an indication of the usefulness and effectiveness of the processes described above. For example, (1) a layer of HSQ having a layer of photoresist removed by exposing wafer 10 to a substantially oxygen free forming gas plasma for four minutes resulted in an effective dielectric constant of approximately 3.00; (2) a layer of HSQ exposed to a solvent used to remove organic and inorganic substances without substantially affecting metallic materials, resulted in an effective dielectric constant of 7.47; and (3) the same HSQ layer as in (1) having a layer of photoresist removed with a substantially oxygen free plasma, followed by the same solvent wash as in (2), resulted in an effective dielectric constant of 3.05. Thus, the solvent wash per (2), that alone degraded the dielectric layer, was protected by physical/chemical changes to the exposed dielectric

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surface resulting from the application of the substantially oxygen free plasma used to remove photoresist.

Similar effective results may be obtained using the disclosed process, however the above exemplary results should not be considered limiting. A number of different plasmas may be used, having forming gasses that include but are not limited to substantially O₂-free, N₂ plus approximately 4% H₂, low O₂ (less than 5% O₂), low O₂ plus H₂ plus approximately 4% N₂, and other suitable forming gasses. Furthermore, wafer 10 may be exposed to the plasma for a variety of times, for example, the exposure times may range from about 30 seconds to about ten minutes. Thus, exposure times are dependent on photoresist thickness, plasma composition, plasma temperature, and other controllable and uncontrollable factors. However, one of ordinary skill in the art could easily find a suitable combination of low-O₂ or non-O₂ plasma and exposure time without undue experimentation. Solvents used in the washing process are well known to those of ordinary skill in the art and all come from a family of solvents that is effective at dissolving organic and inorganic substances without substantially affecting metallic materials. It is well known to those of ordinary skill in the art to use solvents that are compatible with the types of materials that are being removed and those that are intended to be unaffected.

The method and apparatus provide a means to remove photoresist from low-k materials such that the forming gas plasma does not significantly impact the value of the dielectric constant (k). Further, providing trace amounts of O₂ in the plasma forming gas increases the ashing rate. Further still, the low O₂ or O₂- free plasma creates a protective layer to resist solvent attack to the dielectric layers.

It is understood that while the detailed drawings and examples given describe preferred exemplary embodiments of the present invention, they are for the purposes of illustration only. The method and apparatus of the invention is not limited to the precise details and conditions disclosed. For example, it is not limited to the specific plasmas or low-k dielectric materials but only to their specific characteristics such as providing limited low-k dielectric layer degradation and providing the appropriate insulating characteristics respectively. Further, the method and apparatus are not limited to the damascene structure shown, rather the method and apparatus may be applied to a subtractive metal interconnect structure, or any other applicable structures. Various changes may be made to the details disclosed without departing from the spirit of the invention, which is defined by the following claims.

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Claims

1. A method of photoresist removal from an integrated circuit wafer, comprising:

exposing the wafer to a plasma, having a forming gas substantially free of oxygen, to remove at least a portion of the photoresist from the integrated circuit wafer;
removing any remaining portion of the photoresist from the wafer using a solvent; and
degassing the integrated circuit wafer.
2. The method of photoresist removal of Claim 1, wherein the forming gas of the plasma is up to about 20% combined hydrogen gas (H₂) and nitrogen gas (N₂).
3. The method of photoresist removal of Claim 2, wherein the exposing step is carried out for 30 seconds to 10 minutes.
4. The method of photoresist removal of Claim 1, wherein the forming gas of the plasma includes hydrogen gas (H₂), nitrogen gas (N₂), and carbon tetrafluoride (CF₄).
5. The method of photoresist removal of Claim 1, wherein the photoresist is removed after etching at least one via.
6. The method of photoresist removal of Claim 5, wherein a protective layer is created on at least one insulative layer exposed in the at least one via.
7. The method of photoresist removal of Claim 1, wherein the photoresist overlies a low-k dielectric layer.
8. A method of photoresist removal from an integrated circuit wafer, comprising:

providing an integrated circuit wafer having a layer of photoresist overlying a dielectric stack;
and
placing the integrated circuit in a substantially pure plasma, to remove the photoresist from the wafer.
9. The method of photoresist removal of Claim 8, wherein the forming gas of the substantially pure plasma contains less than 5 percent of oxygen gas (O₂).
10. The method of photoresist removal of Claim 8, wherein the dielectric stack is at least partially hydrogen silsesquioxanes (HSQ).
11. The method of photoresist removal of Claim 8, wherein the dielectric stack is at least partially benzocyclobutene (BCB).
12. The method of photoresist removal of Claim 8, wherein the dielectric stack is at least partially spin on glass (SOG).

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13. The method of photoresist removal of Claim 8, wherein the forming gas of the substantially pure plasma is up to 20% combined hydrogen gas (H₂) and nitrogen gas (N₂) and the integrated circuit is exposed to the plasma for a period of approximately 4-10 minutes.
14. The method of photoresist removal of Claim 13, wherein the photoresist layer is less than 1 micrometer (μm).
15. The method of photoresist removal of Claim 8, further comprising:

cleaning off the remaining photoresist from the dielectric stack; and
degassing the wafer.
16. The method of photoresist removal of Claim 15, wherein the degassing process includes exposing the integrated circuit to at least one of a high temperature and a vacuum.
17. An integrated circuit comprising:

a dielectric stack having a first insulative layer, a second insulative layer and a third insulative layer, the second insulative layer being a low-k dielectric layer between the first insulative layer and the third insulative layer,
wherein a via extends through the dielectric stack, wherein lateral sides of the second layer of the dielectric stack include a protective layer.
18. The method of photoresist removal of Claim 17, wherein the protective layer is substantially resistant to solvent attack.
19. The integrated circuit of Claim 18, wherein at least one of the first layer and the third layer is an oxide layer.
20. The integrated circuit of Claim 7, wherein the protective layer is formed by exposing the integrated circuit to a substantially pure plasma.

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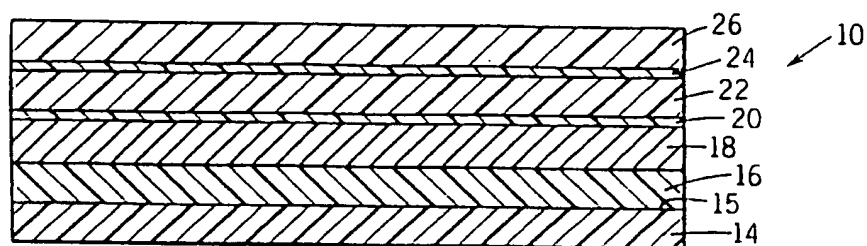


FIG. 1

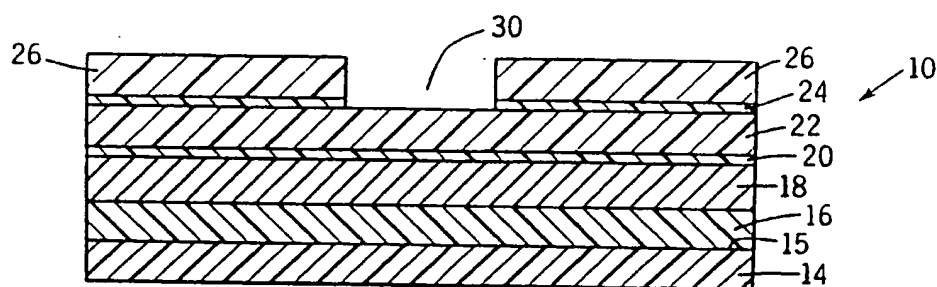


FIG. 2

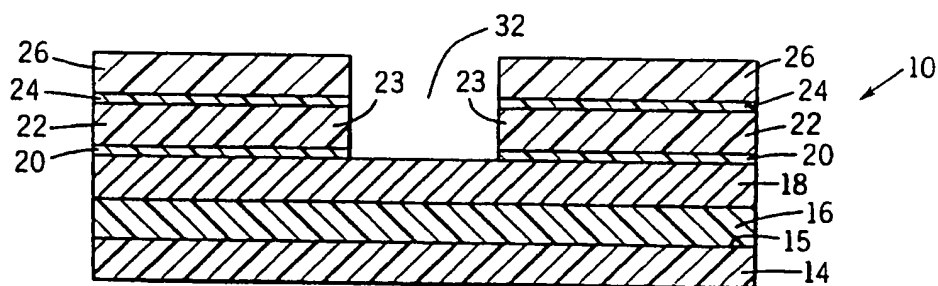


FIG. 3

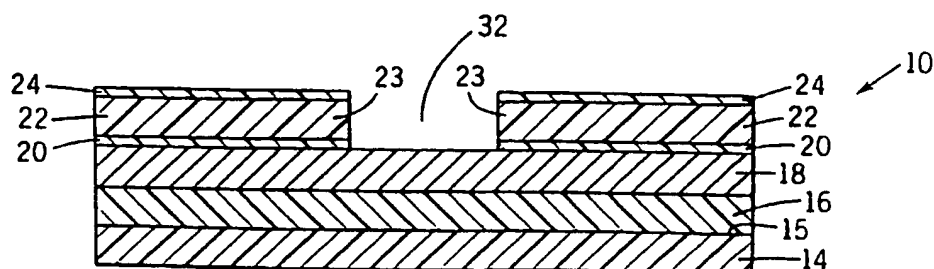


FIG. 4

INTERNATIONAL SEARCH REPORT

Inter. Appl. Application No
PCT/US 00/06603

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G03F7/42 H01L21/311

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L G03F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

INSPEC, EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	LOUIS D ET AL: "Post etch cleaning of low-k dielectric materials for advanced interconnects: characterization and process optimization" MICROELECTRONIC ENGINEERING, vol. 41-42, March 1998 (1998-03), pages 415-418, XP004111746 Elsevier, Netherlands ISSN: 0167-9317	8-10
Y	the whole document	1,5,7, 15,16
Y	WO 99 31725 A (ADVANCED MICRO DEVICES INC) 24 June 1999 (1999-06-24) page 4, line 32 -page 5, line 37 --- -/--	1,5,7, 15,16

☒ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

* Special categories of cited documents:

- *A* document defining the general state of the art which is not considered to be of particular relevance
- *E* earlier document but published on or after the international filing date
- *L* document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
- *O* document referring to an oral disclosure, use, exhibition or other means
- *P* document published prior to the international filing date but later than the priority date claimed

T later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

X document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

Y document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

Z document member of the same patent family

Date of the actual completion of the international search

4 July 2000

Date of mailing of the international search report

13. 11. 2000

Name and mailing address of the ISA

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Köpf, C

INTERNATIONAL SEARCH REPORT

Inter. Appl. Application No.
PCT/US 00/06603

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	NGUYEN D ET AL: "A forming gas resist strip process for use with non-etchback low k spin-on polymers" PROCEEDINGS THIRTEENTH INTERNATIONAL VLSI MULTILEVEL INTERCONNECTION CONFERENCE (VMIC), SANTA CLARA, CA, USA, 18 - 20 June 1996, page 147, XP000923061	8,9,12
A	the whole document	1,2,5,7
X	US 5 795 831 A (NAKAYAMA IZUMI ET AL) 18 August 1998 (1998-08-18)	8,9
A	column 4, line 37 -column 5, line 8	1,2,4,5, 13
X	EP 0 304 068 A (FUJITSU LTD) 22 February 1989 (1989-02-22)	8,9
A	the whole document	1
P,X, L P,A	US 6 030 901 A (HOPPER DAWN ET AL) 29 February 2000 (2000-02-29) L: Priority column 3, line 60 -column 6, line 36	8,9,11 1,5,7,10

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 00/06603**Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)**

This International Search Report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the International Application that do not comply with the prescribed requirements to such an extent that no meaningful International Search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this International Search Report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this International Search Report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this International Search Report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1-16

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest.
- ☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

International Application No. PCT/US 00/06603

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. Claims: 1-16**Optimization of photoresist removal process**

The prior art document (D1) by D. Louis et al, Microelectronic Engineering 41/42 (1998) pp. 415-418, discloses the removal of photoresist after via etching in a dielectric stack (TEOS/HSQ/TEOS) using H₂/N₂ forming gas plasma and subsequent solvent cleaning.

From the comparison of D1 and the application, the new features of the first invention (claims 1-16) considered as "special technical features" of the first invention according to Rule 13(2) PCT, are the specific gas composition and a degassing step after solvent cleaning.

The objective problem solved by these features can be formulated as the optimization of a known etching process (i.e. with respect to gas composition and the removal of final residues after solvent cleaning).

2. Claims: 17-20**Via sidewall protection**

The prior art document D1 discloses a dielectric stack comprising a HSQ low-dielectric constant layer sandwiched between two TEOS layers and via holes etched in the dielectric stack.

From the comparison of D1 and the application, the new feature of the second invention (claims 17-20) considered as "special technical feature" of the second invention according to Rule 13(2) PCT, is a protective layer on lateral sides of the second dielectric layer.

The objective problem solved by this feature can be formulated as the protection of a via hole sidewall etched in a certain dielectric layer.

INTERNATIONAL SEARCH REPORT

Information on patent family members

Inter. .onal Application No

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